Abstract of the Disclosure:

It is possible to read out data in accordance with a read-out address from memory cells via bit lines and primary sense amplifiers. Each secondary sense amplifier is assigned a group of primary sense amplifiers. It is possible for the primary sense amplifiers of a group to be connected to one of the secondary sense amplifiers in each case via switching devices in order to apply the datum from one of the primary sense amplifiers to the assigned secondary sense amplifier via the switching device selected by the read-out address. For reading out data, a test control unit is provided to connect some of the switching devices in parallel depending on a test mode signal and depending on a read-out address, so that in each case one of the group of primary sense amplifiers is connected to the assigned secondary sense amplifiers.

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